CHIPMOS TECHNOLOGIES BERMUDA LTD
Form 6-K
October 04, 2010

SECURITIES AND EXCHANGE COMMISSION

Washington, DC 20549

FORM 6-K

REPORT OF FOREIGN PRIVATE ISSUER

PURSUANT TO RULE 13a-16 OR 15d-16 OF

THE SECURITIES EXCHANGE ACT OF 1934

For the month of October, 2010

ChipMOS TECHNOLOGIES (Bermuda) LTD.

(Translation of Registrant s Name Into English)

No. 1, R&D Rd. 1, Hsinchu Science Park

Hsinchu, Taiwan

Republic of China

(Address of Principal Executive Offices)

(Indicate by check mark whether the registrant files or will file annual reports under cover of Form 20-F or Form 40-F.)

Form 20-F x Form 40-F ¨

(Indicate by check mark whether the registrant by furnishing the information contained in this form is also thereby furnishing the information to the Commission pursuant to Rule 12g3-2(b) under the Securities Exchange Act of 1934.)

Yes ¨ No x

(If Yes is marked, indicate below the file number assigned to the registrant in connection with Rule 12g3-2(b): 82-____ .)

SIGNATURES

Pursuant to the requirements of the Securities Exchange Act of 1934, the registrant has duly caused this report to be signed on its behalf by the undersigned, thereunto duly authorized.

ChipMOS TECHNOLOGIES (Bermuda) LTD.
(Registrant)

Date: October 4, 2010

By /S/ S. J. Cheng
Name: S. J. Cheng
Title: Chairman & Chief Executive Officer

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ChipMOS ANNOUNCES ITS PLANNING INTO 12-INCH WAFER GOLD BUMPING

Hsinchu, Taiwan, October 4, 2010 ChipMOS TECHNOLOGIES (Bermuda) LTD. (Nasdaq: IMOS) today announced the expansion of its wafer gold bumping capabilities in Taiwan into 12-inch, high performance gold bumping production. In anticipation of the expected demand for 12-inch gold-bumping production, the Company plans to add a new, 12-inch gold bumping production line. ChipMOS currently expects facility and equipment setup of its 12-inch gold bumping line to be completed by the end of 2010 and the line will be ready for production at capacity of approximately 4,000 wafers per month on top of the Company s current 8-inch/6-inch gold bumping capacities, which are the current mainstream in driver IC manufacturing. By the end of the third quarter of 2011, the 12-inch gold bumping capacity will ramp up to approximately 10,000 wafers per month.

The decision to expand our high-performance, gold bumping capacity was driven by increasing demand for product applications, such as those used by smartphones, noted S.J. Cheng, Chairman and Chief Executive Officer of ChipMOS. We believe this added capacity will better enable us to capture business opportunities in high resolution mobile display product segment. As an added bonus, we will also be able to utilize the 12-inch wafer gold bumping line for 8-inch wafer gold bumping production in order to address anticipated 8-inch capacity shortage. Importantly, since this line expansion was already factored into our capex plans as discussed in the most recent investor conference call, it will not result in any increase to our budget.

The Company s investment in 12-inch gold bumping capability is designed to meet its customers requirements to adopt 12-inch wafer manufacturing for next generation, one-chip-solution display driver products, which are primarily used in small display panels for mobile applications, including smartphones. Resolution has increased significantly in small display panels, requiring the density of integrated buffer frame memory in the one-chip-solution display driver to increase proportionally to support the multi-functionality of the IC. The result of which is a dramatically enlarged die size of the driver IC. The advantage of employing 12-inch wafer manufacturing technology is the ability to keep the display driver die size small by migrating into finer geometry, while decreasing manufacturing costs per chip via throughput enhancement at the same time. In addition, ChipMOS plans to migrate its existing 8-inch RDL (Re-Distribution Layer) capability into 12-inch together with this capacity expansion and provide more MCP (Multi-Chip Package) assembly flexibilities for mobile/niche DRAM or flash customers.

About ChipMOS TECHNOLOGIES (Bermuda) LTD.:

ChipMOS (http://www.chipmos.com) is a leading independent provider of semiconductor testing and assembly services to customers in Taiwan, Japan, and the U.S. With advanced facilities in Hsinchu and Southern Taiwan Science Parks in Taiwan and Shanghai, ChipMOS and its subsidiaries provide testing and assembly services to a broad range of customers, including leading fabless semiconductor companies, integrated device manufacturers and independent semiconductor foundries.

Forward-Looking Statements

Certain statements contained in this announcement may be viewed as forward-looking statements within the meaning of Section 27A of the U.S. Securities Act of 1933, as amended, and Section 21E of the U.S. Securities Exchange Act of 1934, as amended. Such forward-looking statements involve known and unknown risks, uncertainties and other factors, which may cause the actual performance, financial condition or results of operations of the Company to be materially different from any future performance, financial condition or results of operations implied by such forward-looking statements. Further information regarding these risks, uncertainties and other factors is included in the Company s most recent Annual Report on Form 20-F filed with the U.S. Securities and Exchange Commission (the SEC) and in the Company s other filings with the SEC.